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10/605,015	09/01/2003	Chih-Chin Chang	ADTP0094USA	2014

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EXAMINER
ARENA, ANDREW OWENS

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,015	CHANG ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: the amendment to claim 1 includes grammar errors:

"electrically connecting to" is awkward and should read "electrically connects to";

"disconnecting to" is awkward and should read "does not electrically connect to".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant regards as the invention. Evidence that claim 11 fails to correspond in scope with that which applicant regards as the invention can be found in the specification. In that paper, applicant has indicated "a periphery circuit area 104" and "a capacitor area 106...in the pixel array area 103" (¶19 ln 11-12; Fig 3), whereas claim 11 contrarily recites "the capacitor structure is disposed in the periphery circuit area".

4. For art-based rejection purposes, the area in which the capacitor is located is regarded as the periphery circuit area.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over of the admitted prior art – hereinafter APA – in view of Ikeda at al. (US 5,182,661) – hereinafter Ikeda.

7. Regarding claim 1, APA discloses (Fig 2) a capacitor structure comprising:

a substrate (32);

a first conductive layer (48) disposed on the substrate;

a first insulating layer (52) disposed on the first conductive layer;

a second conductive layer (54) disposed on portions of the first insulating layer;

a second insulating layer (56) disposed on portions of the second conductive layer and the first insulating layer,

wherein the capacitor structure electrically [connects] to a thin film transistor (TFT: 38) and the first conductive layer [does not connect] to a gate (44) of the TFT in a display;

but differs from the claimed invention in not disclosing “a third conductive layer”, “a third insulating layer”, a “fourth insulating layer”, or a “fifth insulating layer”.

Ikeda discloses a capacitor structure (Fig 4B) with:

a third conductive layer (62) disposed on portions of the second insulating layer and electrically connecting to the first conductive layer (col 5 ln 30) through at least one first contact hole (64), the first contact hole being adjacent to the second conductive layer (64 adjacent to 60 by way of 44);

a third insulating layer (46) disposed on the third conductive layer and the second insulating layer; and

a fourth conductive layer (22; portion right of 66) disposed on the third insulating layer and electrically connecting to the second conductive layer (col 5 ln 33-37) through at least one second contact hole (66) and a fifth conductive layer (22; portion left of and inside of 66).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify APA by utilizing the stacked capacitor structure of Ikeda for the storage capacitor of APA; at least for large capacitance.

8. Regarding claim 2, APA discloses (Fig 2) the substrate (32) comprises a glass substrate (¶6 ln 7).

9. Regarding claim 3, APA differs from the claimed invention only in not expressly disclosing the first conductive layer is a polysilicon layer, but does disclose the first conductive layer is formed on the same layer (46) as the polysilicon (¶6 ln 14-16) gate (44) of the TFT (38). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first conductive layer of APA be a polysilicon layer; at least for ease of manufacture.

10. Regarding claim 4, APA discloses (Fig 2) the first insulating layer (52) comprises a silicon oxide layer (¶8 ln 2).

11. Regarding claim 5, APA as modified by Ikeda discloses both of the second conductive layer and the third conductive layer comprise a metal layer (Ikeda: col 5 ln 15-16 and 22).

12. Regarding claim 6, APA as modified by Ikeda discloses the metal layer comprises a chrome layer (Ikeda: col 5 ln 15).

13. Regarding claim 7, APA as modified by Ikeda discloses (Ikeda: Fig 4) the fifth conductive layer is disposed in the second contact hole (portion of 22 in 66) to electrically connect the fourth conductive (22) layer and the second conductive (60) layer (col 5 ln 33-35).

14. Regarding claim 8, APA as modified by Ikeda discloses (Ikeda: Fig 4) the third conductive layer (62) and the fifth conductive layer (22) are not connected (Fig 4B).

15. Regarding claim 9, APA discloses (Fig 2) the substrate is an array substrate of a liquid crystal display (LCD 30; ¶6 ln 4), a pixel array area (33; ¶6 ln 8) is included on a surface of the substrate,

and APA as modified by Ikeda further discloses (Ikeda: Fig 4): and the fourth conductive layer is electrically connected to a thin film transistor (TFT 14) in the pixel array area through the fifth conductive layer (22 to 34 by way of 36; col 3 ln 44-46).

16. Regarding claim 10, APA discloses the capacitor structure is disposed in the pixel array area (33) on the substrate to be used as a storage capacitor (42; ¶6 ln 14).

17. Regarding claim 11, APA discloses the substrate is an array substrate of a liquid crystal display (LCD 30; ¶6 ln 4), a periphery circuit area (34; ¶6 ln 8-9) is included on a surface of the substrate, and the capacitor structure is disposed in the periphery circuit area on the substrate (in view of the 35 USC 112 ¶2 indefiniteness of claim 11).

18. Regarding claim 12, APA discloses the second insulating layer (56) comprises a silicon nitride layer (¶8 ln 5).

19. Regarding claim 13, APA as modified by Ikeda discloses (Ikeda: Fig 4B) the first contact hole (64) is disposed in the first insulating layer (42) and the second insulating layer (44), and the first contact hole exposes portions of the first conducting layer (68; col 5 ln 29-33).

20. Regarding claim 14, APA as modified by Ikeda discloses (Ikeda: Fig 4B) the third insulating layer comprises a silicon nitride layer (col 5 ln 25-26).

21. Regarding claim 15 APA as modified by Ikeda discloses (Ikeda: Fig 4B) the fourth conductive layer comprises an indium tin oxide (ITO) layer (col 5 ln 10-11).

22. Regarding claim 16, APA as modified by Ikeda discloses (Ikeda: Fig 4B) the second contact hole (66) is disposed in the second insulating layer (44), and the second contact hole exposes portions of the second conductive layer (60; col 5 ln 35-37).

23. Regarding claim 17, APA as modified by Ikeda discloses (Ikeda: Fig 4B) the first conductive layer, the first insulating layer, and the second conductive layer form a first capacitor; the second conductive layer, the second insulating layer, and the third conductive layer form a second capacitor; and the third conductive layer, the third insulating layer, and the fourth conductive layer form a third capacitor (this is all inherent

in the structure of Fig 4B, there must be a capacitance between each pair of conductors spaced by an insulator).

24. Regarding claim 18, APA as modified by Ikeda discloses (Ikeda: Fig 4B) the second conductive layer and the fourth conductive layer are used as one electrode of the capacitor, but does not disclose the polarity, and the second conductive layer and the fourth conductive layer are electrically connected by the fifth conductive layer through the second contact hole; the first conductive layer and the third conductive layer are used as the other electrode of the capacitor, but does not disclose the polarity, and the first conductive layer and the third conductive layer are electrically connected through a first contact hole filled with the third conductive layer.

It is apparent that the capacitor can be connected such that a given electrode can have either polarity, depending on the polarities desired for other components of the TFT-LCD device. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to connect the capacitor with the polarities as claimed, since there is no obvious advantage of either particular choice.

25. Regarding claim 19, APA as modified by Ikeda discloses (Ikeda: Fig 4B) utilizing multi-layered conductive layers as multi-layered electrode plates (68, 60, 62, 22) to form at least two stack capacitors (there must be a capacitance between each pair of conductors spaced by an insulator).

26. Regarding claim 20, APA as modified by Ikeda discloses (Ikeda: Fig 4B) the capacitance value of the capacitor is equal to the capacitance value of an equivalent

capacitor including the first capacitor, the second capacitor, and the third capacitor connected in parallel with one another (inherent in the structure of Fig 4B).

27. Regarding claim 21, APA discloses (Fig 2) the gate (44) and the capacitor (42) are in the pixel array area (33).

Response to Arguments

28. Applicant's arguments filed on 10/31/2005 have been considered, but are moot in view of the new ground(s) of rejection.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOA
03/04/2006

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